Density profiles and electrical properties of thermally grown oxide nanofilms on *p*-type 6H–SiC(0001)

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Thermally grown silicon oxide films on *p*-type 6H–silicon carbide substrate under different oxidation and nitridation conditions have been characterized by x-ray reflectivity technique. An electron density profile obtained from the analysis of the x-ray reflectivity data shows that the thickness, density of the oxide film, and structure of the oxide-SiC interface strongly depend on the different growth conditions. In particular, the density of the oxide film for all samples other than that grown in NO is found to be much lower and also not fixed within. It is maximum at the interface and gradually decreases toward the top in all samples except for the sample grown in O_2 followed by NO nitridation. For the latter, a very low density at the interface region has been observed. The sample grown in NO shows the best performance in capacitance–voltage characteristic and reliability studies suggesting that the bad performance of the oxide grown on the *p*-type SiC system as metal–oxide–semiconductor devices, is *mainly* linked to the low-density oxide film and can be overcome under proper growth condition. © *2004 American Institute of Physics*.
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Silicon carbide (SiC) is the semiconductor of choice for high-temperature, high-power, and high-frequency devices because of its large band gap. The ability to grow thermal oxides on SiC gives significant advantages over other compound semiconductors and also makes it compatible with other silicon technologies. However, the performance of metal–oxide–semiconductor (MOS) devices on SiC has been limited by the poor quality of oxide and the oxide–SiC interface.[1] Previous results also indicated that the quality of SiO_2, thermally grown on a *n*-type SiC substrate, is comparable to that grown on Si, but thermally grown oxide on *p*-type SiC exhibits poorer electrical behavior.[2,3] Researchers also investigated the effects of preoxidation cleaning,[4] postannealing in argon,[5] and reoxidation[6] on interface properties of SiO_2/SiC systems. Nitridation of already existing oxide in a NO ambient led to better interface quality, but nitridation in N_2O produced poorer oxide quality.[7] Oxide grown in a pure N_2O environment also showed better interface quality and reliability.[8] Besides electrical characterization, the estimation of density of the thermally grown oxide using x-ray reflectivity (XRR) technique also plays an important role in understanding and characterizing the interface in a direction to improve the performance of SiO_2/SiC MOS devices.

Surface sensitive XRR is an extremely powerful technique to study the morphology of a thin film.[9,10] It provides an electron density profile (EDP) of the film,[11,12] from which it is possible to extract the film thickness, the mass density of the film along the growth direction, and the interfacial structure. In this letter, we have utilized an XRR technique to study the morphology of oxide film, thermally grown under different oxidation and nitridation conditions on a *p*-type SiC wafer. The electrical properties of the corresponding MOS structure are then analyzed in the light of the obtained morphology, which brings out the correlation of oxide reliability with the morphology for a device application.

A Si-faced *p*-type 6H–SiC(0001) wafer, manufactured by CREE Research, was used here. A 5 μm thick SiC epitaxial layer was grown on heavily doped substrates. The doping level of the epitaxial layer was 4×10^{15} cm^{-3}. The wafer was cut into five pieces to grow oxide layers. Each piece (of size ~1 cm$\times1$ cm) was cleaned using a Radio Corporation of America technique, and finally HF was used to remove the native oxide film. Pieces of wafer were then loaded into a quartz furnace at 800 °C and oxidation was performed at a temperature of 1100 °C using different gases for different durations. Growth conditions for five oxide samples, denoted as A–E, are indicated in Table I. All the pieces were then annealed in N_2 at 1100 °C for 30 min. For electrical measurements, aluminum was thermally evaporated, and then patterned as a gate electrode of MOS capacitors. The area of each capacitor was 1.8×10^{-4} cm^2. No postmetal annealing was performed, to avoid masking the defects created during oxidation and/or nitridation. SiO_2/SiC interface-state density was studied by high-frequency capacitane–voltage (C–V) measurement after light illumination at deep depletion. The device reliability was studied under high-field stress (-7 MV/cm) on the MOS device with the capacitor biased in accumulation. All measurements were carried out at a frequency of 1 MHz at room temperature under dark and electrically shielded conditions. The XRR measurements of all the samples were carried out using a laboratory x-ray source.[11]

XRR data of the oxide grown on SiC wafers are shown in Figs. 1 and 2. Oscillations in all curves are due to the

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TABLE I. Parameters obtained from the analysis of XRR and electrical data of oxide grown *p*-type SiC wafers in different growth conditions.

Sample	Growth condition [gas (time in min)]	t_{ox} (nm)	ρ_a/ρ_p	$\varepsilon_a/\varepsilon_p$	V_{fb} (V)	Q_{ox} ($\times 10^{11}$ cm^{-2})	ΔQ_{ox} ($\times 10^{11}$ cm^{-2})	D_{it} ($\times 10^{11}$cm^{2}eV^{-1})[a]
A	O_2 (210)	11.1	0.65	0.52	−4.37	19.70	22.10	6.18
B	O_2 (210), N_2O(90)	12.7	0.73	0.55	−5.10	23.99	29.40	8.74
C	O_2 (210), NO(90)	12.8	0.80	0.60	−3.85	13.30	15.30	4.67
D	N_2O (360)	12.9	0.74	0.77	−2.60	00.89	01.20	2.39
E	NO (360)	08.8	0.92	0.58	−2.55	00.28	00.35	1.45

[a]Before stress.

presence of thin oxide layer. However, XRR data has been analyzed using Parratt formalism[13] to obtain the EDP including roughness at each interface.[11] Two models were used for the analysis of the data. First, we consider oxide as a single layer and its electron density is the density ($\rho_p \sim 0.71$ Å^{-3}) of perfect SiO_2. Thus, by using the thickness of the oxide layer and roughness at each interface as parameters, the XRR curves were fitted. Dashed lines through the XRR data in Figs. 1 and 2 are the best fit curves for the simple model, and the corresponding roughness convoluted EDP[11] is represented by the dashed lines in the inset. It can be noted that although the simple model cannot predict exactly the experimental XRR curve, it gives an estimate of the thickness (t_{ox}) of the oxide layer (listed in Table I). Table I shows that the value of t_{ox} for samples B, C, and D are almost the same but slightly more than that of sample A. However, the value is quite low for sample E, which may not be the case as discussed later.

To predict the experimental XRR curve better, we have used another model. According to this detailed model, the oxide layer has been divided into a number of slabs[11] and the thickness, electron density (ρ), and roughness of each slab were considered as parameters. Solid lines through the XRR data in Figs. 1 and 2 are the best fit curves for the detailed model, and the corresponding EDP is shown in the inset by solid lines. It can be noted that the electron density of the oxide layer in all samples, other than sample E, is found to be much less compared to that of perfect SiO_2. The electron density is also not fixed within the oxide layer: It gives a maximum at the interface and gradually decreases toward the top in all cases except for sample C. For the latter, a very low electron density at the interface region has been observed. The average electron density (ρ_a) of the oxide layer has been estimated by integrating the electron density over the oxide thickness and dividing it by the thickness. The values of ρ_a normalized with ρ_p, have been tabulated in the Table I. A value of less than 1.0 indicates reduced electron density of the oxide layer. However, the value of ρ_a/ρ_p, for samples B and C increases compared to that of sample A indicating that further use of N_2O and NO during growth filled up some defects or pores in the oxide film. A better density was obtained even for samples grown in a N_2O or NO ambient. However, the best density was observed for the sample grown on NO ambient.

Figure 3 shows the high-frequency *C–V* curves for all MOS structure, where *C* has been normalized with the corresponding maximum value, C_{ox}. The average dielectric constant (ε_a) of the oxide layer of each film has been estimated from C_{ox}, using the value of t_{ox}, obtained from XRR measurement. The value of ε_a, normalized with the value of dielectric constant, $\varepsilon_p(\sim 3.9)$, of perfect SiO_2, has been listed in the Table I. A value of less than 1.0 indicates a reduced

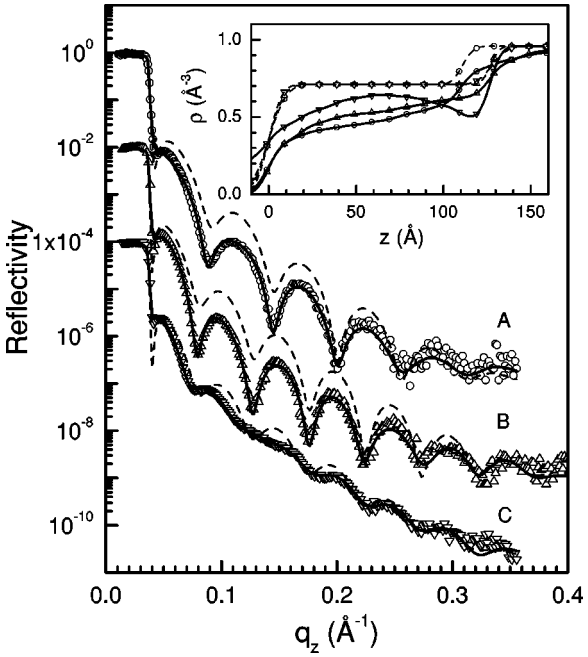

FIG. 1. Measured (symbol) and calculated (dashed and solid lines are for simple and detailed models, respectively) XRR curves of three SiC samples where oxide layers are grown in O_2 (A), O_2 followed by N_2O (B), and NO (C). Curves are shifted vertically for clarity. Inset shows corresponding EDP.

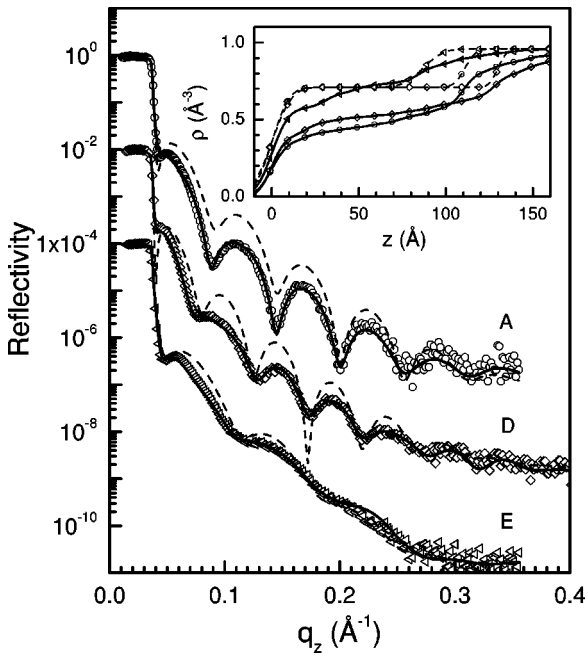

FIG. 2. Measured (symbol) and calculated (dashed and solid lines are for simple and detailed models, respectively) XRR curves of three SiC samples where oxide layers are grown in O_2 (A), N_2O (D), and NO (E). Curves are shifted vertically for clarity. Inset shows corresponding EDP.

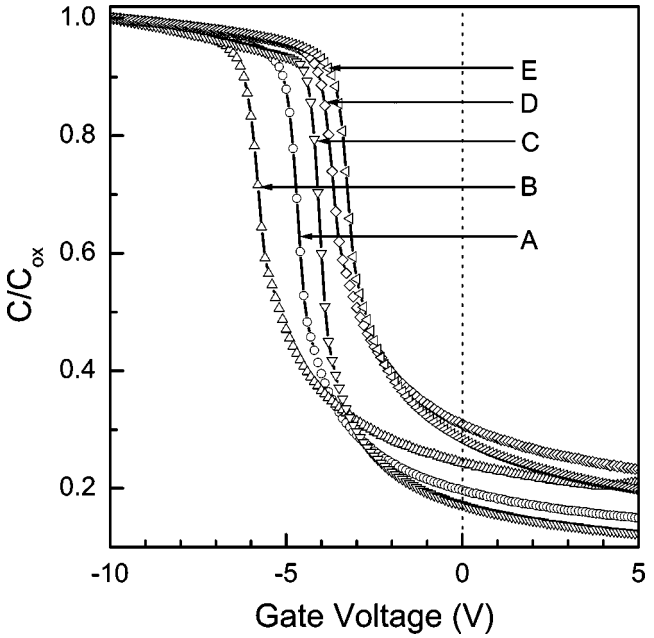

FIG. 3. High-frequency (1 MHz) *C–V* measurements of MOS capacitors fabricated on *p*-type 6H-SiC.

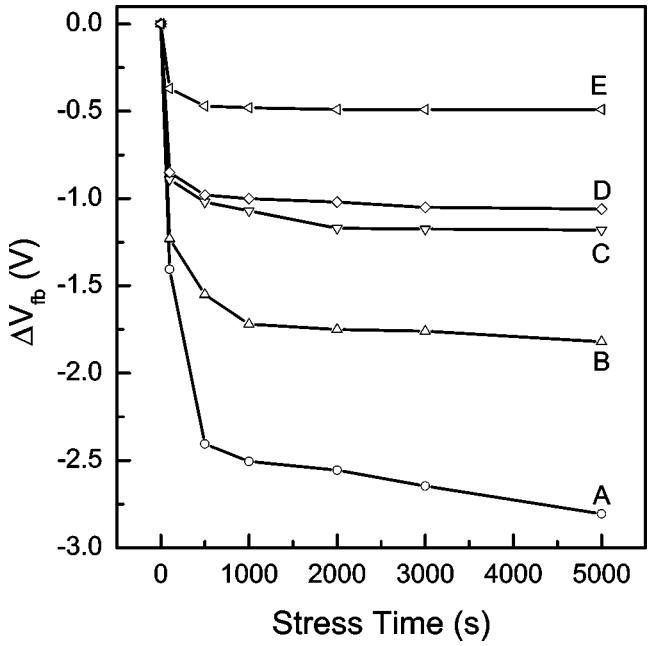

FIG. 4. Flat-band voltage shifts during high-field room-temperature stressing of the devices.

dielectric constant that can be attributed to a porous structure of most thermally grown oxide layers similar to that obtained from the XRR analysis. However, the low value of ε_a, for sample E is due to the small thickness of the oxide film. It is also possible that this thickness is actually a part of total oxide layer ($\sim$ 12.8 nm) and the remaining part is close to the substrate where the increase in density may be due to the nitrogen incorporation. If it is considered as the case, then the value of $\varepsilon_a/\varepsilon_p$ will be 0.84 for sample E. From the $C-V$ curve and flat-band voltage (V_{fb}), the oxide charge (Q_{ox}) and the interface-state density (D_{it}) have also been estimated,[5,14] which are listed in Table I for all samples. A large negative voltage shift indicates the presence of a significant amount of positive charge in the oxide or at the oxide–SiC interface. The minimum V_{fb} for sample E indicates the least oxide charge density. The estimated D_{it} is also found to be the least for the same device. This observation indicates that oxide, grown in pure NO ambient, has the best interface quality. Among the nitrided devices, sample C is found to have exhibited improved V_{fb} and D_{it} values. The improvement is mainly attributed to the incorporation of nitrogen during the use of NO during growth or annealing process.

The V_{fb} shift of all the devices during high-field stress at room temperature is shown in Fig. 4. The negative flat-band shift (ΔV_{fb}) indicates the generation of donorlike interface states and positive oxide charges. A much smaller ΔV_{fb} obtained for NO device indicates a significantly suppressed generation of interface traps and oxide charges. From the observed ΔV_{fb} at 5000 s stress time, an increase in effective oxide charge (ΔQ_{ox}) is estimated. The enhanced hardness of sample E against high-field stress results from the incorporation of nitrogen at on near the SiO_2/SiC interface, formation of Si—N bonds, and replacement of weak Si—O bonds. In the addition, the during 100 s stress time, ΔV_{fb} is mainly linked with pre-existing donorlike interface states and near-interface traps which both are neutral before the stress. In case of sample E, much fewer interface states and oxide traps are observed during first 100 s stress time which is also in good agreement with the data shown in Table I.

In conclusion, oxide nanofilms grown under different oxidation and annealing conditions on *p*-type 6H-SiC surface show low density and reduced dielectric constant due to their porous structure. Both values however increase when the oxide layer grown either in a N_2O or NO ambient, or in O_2 followed by N_2O and NO. For the oxide films grown in NO and O_2 followed NO, these values are even higher. The improvement in the reliability of oxide of these two samples suggests the strong role of density and/or dielectric constant. The sample grown in a NO ambient exhibits the smallest flat-band shift and interface-state density among all the devices. A much better stability of this device under high-field stress is probably due to the incorporation of nitrogen near the SiO_2/SiC interface.

[1] J. W. Palmour, L. A. Lipkin, R. Singh, D. B. Slater, Jr., A. V. Suvorov, and C. H. Carter, Jr., Diamond Relat. Mater. **6**, 1400 (1997).
[2] D. Alok, P. K. McLarty, and B. J. Baliga, Appl. Phys. Lett. **65**, 2177 (1994).
[3] S. Sridevan, P. K. McLarty, and B. J. Baliga, IEEE Electron Device Lett. **17**, 136 (1996).
[4] V. V. Alfans'ev, A. Stesmans, M. Bassler, G. Pensl, M. J. Schulz, and C. I. Harris, Appl. Phys. Lett. **68**, 2141 (1996).
[5] H. Yano, F. Katafuchi, T. Kimoto, and H. Matsunami, IEEE Trans. Electron Devices **46**, 504 (1999).
[6] P. T. Lai, S. Chakraborty, C. L. Chan, and Y. C. Cheng, Appl. Phys. Lett. **76**, 3744 (2000).
[7] S. Dimitrijev, H.-F. Li, H. B. Harrison, and D. Sweatman, IEEE Electron Device Lett. **18**, 175 (1997).
[8] J. P. Xu, P. T. Lai, C. L. Chan, B. Li, and Y. C. Cheng, IEEE Electron Device Lett. **21**, 298 (2000).
[9] A. Gibaud and S. Hazra, Curr. Sci. **78**, 1467 (2000).
[10] *X-ray and Neutron Reflectivity: Principles and Applications*, edited by J. Daillant and A. Gibaud (Springer, Paris, 1999).
[11] S. Kundu, S. Hazra, S. Banerjee, M. K. Sanyal, S. K. Mandal, S. Chaudhuri, and A. K. Pal, J. Phys. D **31**, 73 (1998).
[12] S. D. Kosowsky, P. S. Pershan, K. S. Krisch, J. Bevk, M. L. Green, D. Brasen, L. C. Feldman, and P. K. Roy, Appl. Phys. Lett. **70**, 3119 (1997).
[13] L. G. Parratt, Phys. Rev. **95**, 359 (1954).
[14] D. K. Schroder, *Semiconductor Material and Device Characterization* (Wiley, New York, 1998).